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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/301,284 | 04/28/1999 | SHUICHI TAKAYAMA | NAK1-BG86 | 5392 |

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| EXAMINER | |
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2122 | 13 |

DATE MAILED: 04/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/301,284 | TAKAYAMA ET AL. |
| | Examiner | Art Unit |
| | Ted T. Vo | 2122 |

*-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

1. This action is in response to the communication filed on 1/30/2002.

Claims 1, 11 are amended. Claims 12-48 are canceled. Claims 1-11 are pending in the application.

### *Drawings*

2. The corrected or substitute drawings were received on 1/30/02. Examiner for examination purpose accepts these drawings only.

### *Information Disclosure Statement*

3. The information disclosure statement filed 8/13/1999 fails to comply with the provisions of 1.98(a) and MPEP § 609 because it does not submit an English translation. It should be indicating with quote "abstract" in the content, or providing with full English version. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e).

***Response to Arguments***

4. Applicant's request for reconsideration and arguments have been fully considered but they are not persuasive.

-Regarding the applicant's argument, the claim rejection under 35 USC 112 first paragraph is withdrawn. However, it raises a rejection under 35 USC 112 second paragraph.

- Regarding the applicant's argument and amendment, the claim rejection under 35 USC 102:

-Applicant argues that Christie's program counter (less significant program counter) is not capable of indicating a position of a processing target instruction. Less significant program counter fails to teach second program counter (applicant's feature) for indicating a position of a processing target instruction within the processing packet that is not required to correspond to a byte boundary.

- Examiner respectfully disagrees: Christie program counter is used to indicate a RISC instruction (instruction packet) or X86 instruction. A RISC instruction has four ROPs. Christie's program counter includes 32 bits in which a set of bits (0:3), less significant program counter, positions one of four ROPs (position of processing target instruction). Therefore, the less significant program counters is corresponding to the second counter. With respect to applicant's second program counter described as for indicating a position of processing target instruction within the processing packet, Christie's program less significant program counter uses a set of bits (0:3) to indicate one of four ROPs in a queue, and a set of bits (4:31), more significant program counter, positions a RISC instruction or X86 instruction (processing packet).

Since Christie discloses that 4 bits of less significant represent offset values corresponding to the four ROPs or an X86 instruction (column 10, lines 24-42), this might be referred by applicant's argument as the position to a byte boundary, because the count of X86 instruction is within a circle time. However, in

an embodiment, (column 18, lines 4-23), Christie discloses that the less significant program counter combines a multiplexer, where the multiplexer provides the least significant four bits of potential next decode program counter value; each potential next decode program counter value corresponds to a ROP from the queue. Using this feature, Christie's less program counter is to indicate a position of such a ROP (possessing target instruction) in an instruction set regardless whether the position of the ROP corresponds to the byte boundary.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claimed functionality of claims 10-11 are unclear. Examiner would respectfully request applicant to explain the functionality of claim 10-11. What functions do the claims perform? According the specification page 9, the specification asserts that leftward bit shifting to a value of log2(n) where n is a length of a processing packet in bytes will specify easily a processing address. This description is set as utility to support the claims 10-11. However, it is very vague.

If n=4 the length in byte of a processing packet, then log2(4)=2. Every bit in the first counter is shifted to the left two positions. Assume that value of the first counter is: 86X = 1000 0110

After performing shifting, the new value of the counter is: 18X = 0001 1000

Does 18X specify the address of a processing packet?

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Christie et al., US Patent No. 5,559,975.

As per claim 1:

-Regarding claim limitations:

"*A processor for reading instructions from a memory according to a program counter, and for executing the read instructions, the program counter including a first program counter and a second program counter, the first program counter indicating a storage position of a processing packet in the memory, the processing packet being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary* "

Christie's reference teaches the claim limitations by using (4:31) bits (*first program counter*), named as more significant program counter, to position to a byte boundary of a RISC instruction set or a X86 instruction. The counter increments or branches to the next instruction set of RISC or X86 using a multiplexer 761 (see column 18, lines 24-38).

-Regarding claim limitations:

"*the second program counter indicating a position of processing target instruction in the processing packet regardless of whether the position corresponds to a byte boundary, the processing target instruction being an operation to be executed by the processor* ",

Christie's reference teaches the claim limitations by using a set bit (0:3) (*second program counter*) which is combined with a multiplexer (see column 18, lines 4-23), where the multiplexer provides the least significant four bits of potential next decode program counter value; each potential next decode program counter value corresponds to a ROP from the queue (a queue consists a number of ROPs of an instruction set). Using this feature, Christie's less program counter is to indicate a position of the ROP (possessing target instruction) in the X86 instruction regardless whether the position corresponds to the byte boundary.

As per claim 2:

-Regarding claim limitations of claim 2, Christie teaches further claim limitations "first program counter updating and second program counter updating" using the incrementer, adders, and multiplexers (see column 18, lines 4-23, and lines 24-38).

As per claim 3:

-Regarding claim limitations of claim 3, claim 3 is inherent from relative address values used in a program when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38) to perform adding that sets the address of the relative address value in the program counters. To perform the adding a relative value included in an instruction, Christie discloses that in a branch, an instruction is fetched and decoded. The counter identifies the next address of the target instruction, and uses adders, selectors, to form the next address (this mechanism is provided in the discussion column 18, lines 4-38).

As per claim 4:

-Regarding claim limitations of claim 4, claim 4 manipulates a calculation performed by adders in the first counter in the second counter. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 5:

-Regarding claim limitations of claim 5, claim 5 manipulates a calculation performed by adders in the first counter in the second counter corresponding to the functionality of claim 4. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 6:

-Regarding claim limitations of claim 6, claim 6 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 7:

-Regarding claim limitations of claim 7, claim 7 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 8:

-Regarding claim limitations of claim 8, claim 8 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 9:

-Regarding claim limitations of claim 9, claim 9 is inherent from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 10:

-Regarding claim limitations of claim 10, given the broadest interpretation in light of specification, the specification asserts that with the construction of bit shifting given in the first program counter the value by log2(n) in the leftward direction will easily specify a processing packet in the memory. Christie discloses the more program counter (4:30) indicates an address of an X86 or RISC instruction set which has 4 ROPs. Christie uses an incrementer, or a multiplexer which adds the value of the more significant program counter to the next address value of the instruction set (see column 18, lines 23-38).

As per claim 11:

-Regarding claim limitations of claim 11, functionality claim 11 is inherent in registers, read/write address buffers, cache, and fetch mechanism used to store data as shown in Christie's figures (Figures 1A...).

***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Morse, can be reached on (703) 308-4789.

The fax phone numbers for this Group are:

Official: (703) 746-7239.

After Final: (703) 746-7238.

Non-Official: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TTV
April 12, 2002

GREGORY MORSE
SUPERVISORY PATENT EXAMINER
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